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Pat.Abs.of Jp.Vol.7,No.255(E210),12/11/83,page133, SUWA SEIKO SHA and JP58-141572

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INT CL[6] H01L
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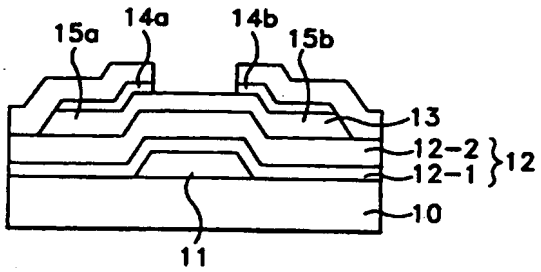
(54) Gate insulation layers for thin film transistors

(57) A thin film transistor comprises a gate electrode 11, an active layer 13, and a gate insulating layer 12 comprising a diamond-like carbon layer 12-1, formed between the gate electrode and the active layer. Diamond-like carbon with a good insulating property is used as a gate insulating layer of the TFT, so a production yield of a TFT employing the diamond-like carbon increases. The carbon layer 12-1 is deposited by plasma enhanced C.V.D of a gas such as CH_4, C_2H_6, C_2H_2 or C_3H_8. A silicon nitride layer 12-2 is also deposted on the carbon layer enhanced C.V.D and the active layer of hydrogenated amorphous silicon, amorphous silicon or polysilicon is deposited on the silicon nitride layer.

FIG.1



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The title has been truncated. The full title is as follows. Gate insulating layer having diamond-like carbon and thin film transistor employing the same and process for manufacturing gate insulating layer and thin film transistor

FIG.1

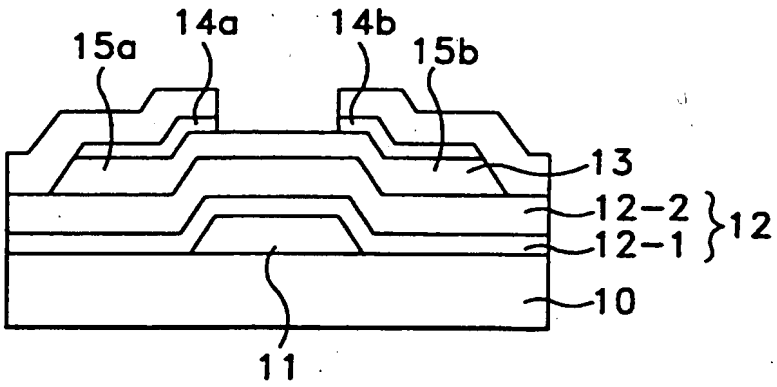


FIG.2

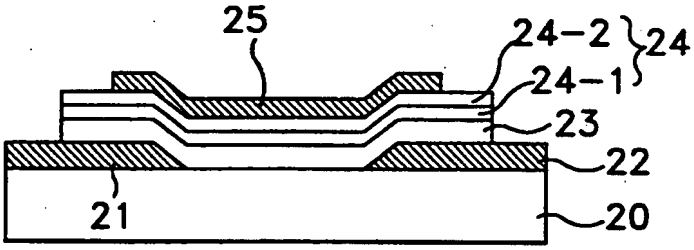


FIG.3

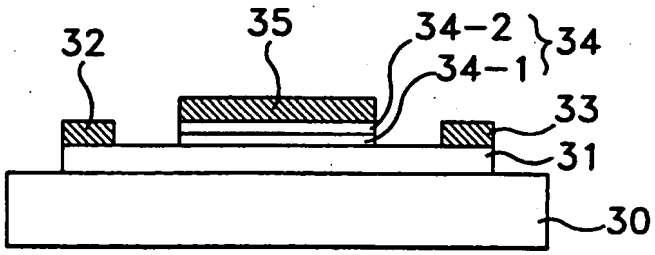


FIG.4

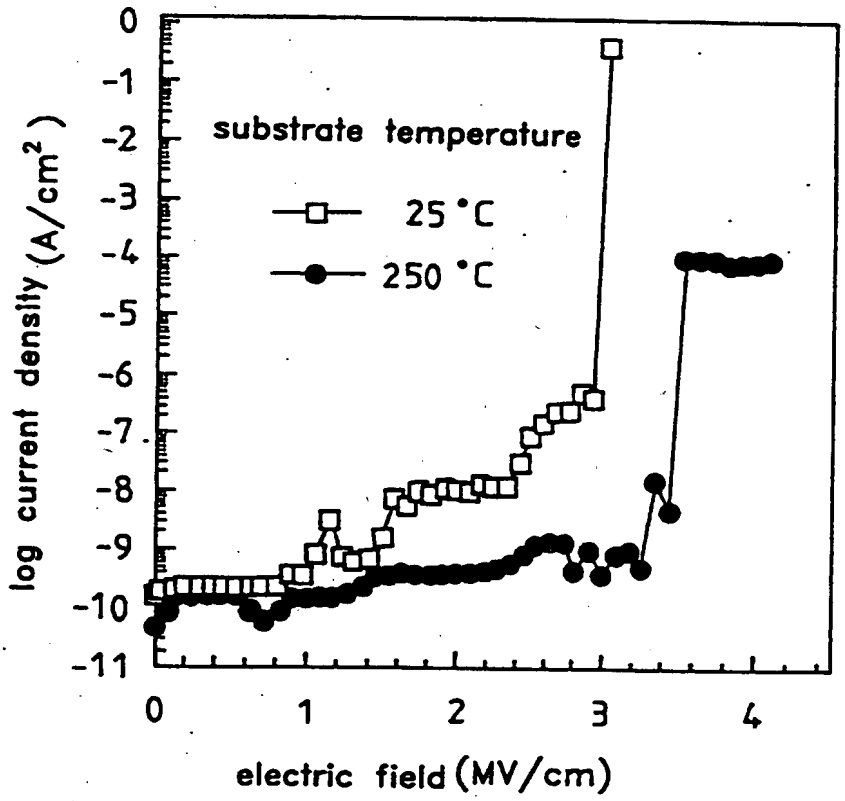

0
-1
-2
-3
-4
-5
-6
-7
-8
-9
-10
-11
log current density (A/cm²)
substrate temperature
25 °C
250 °C
0
1
2
3
4
electric field (MV/cm)

FIG.5

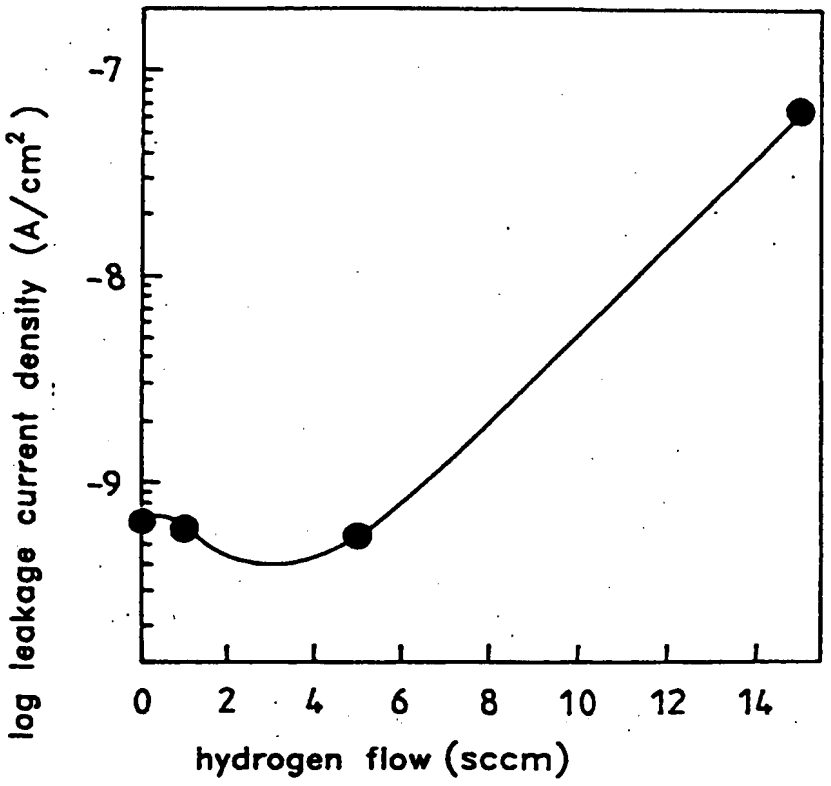

log leakage current density (A/cm²)
-7
-8
-9
0
2
4
6
8
10
12
14
hydrogen flow (sccm)

FIG.6

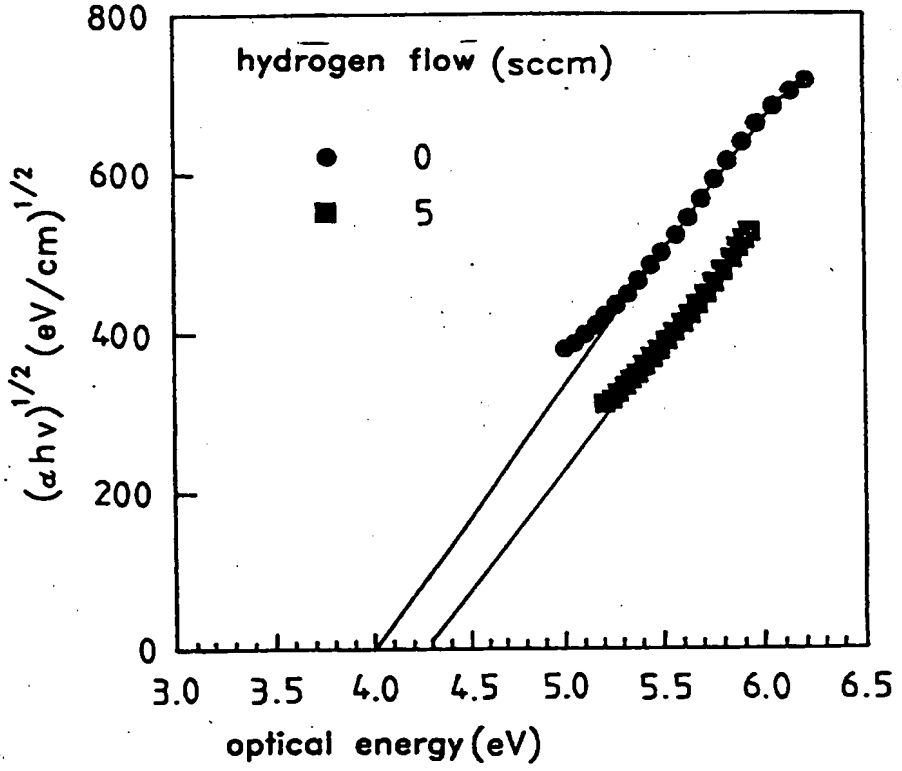

800
600
400
200
0
hydrogen flow (sccm)
0
5
$(\alpha h\nu)^{1/2}(eV/cm)^{1/2}$
3.0
3.5
4.0
4.5
5.0
5.5
6.0
6.5
optical energy (eV)

FIG.7

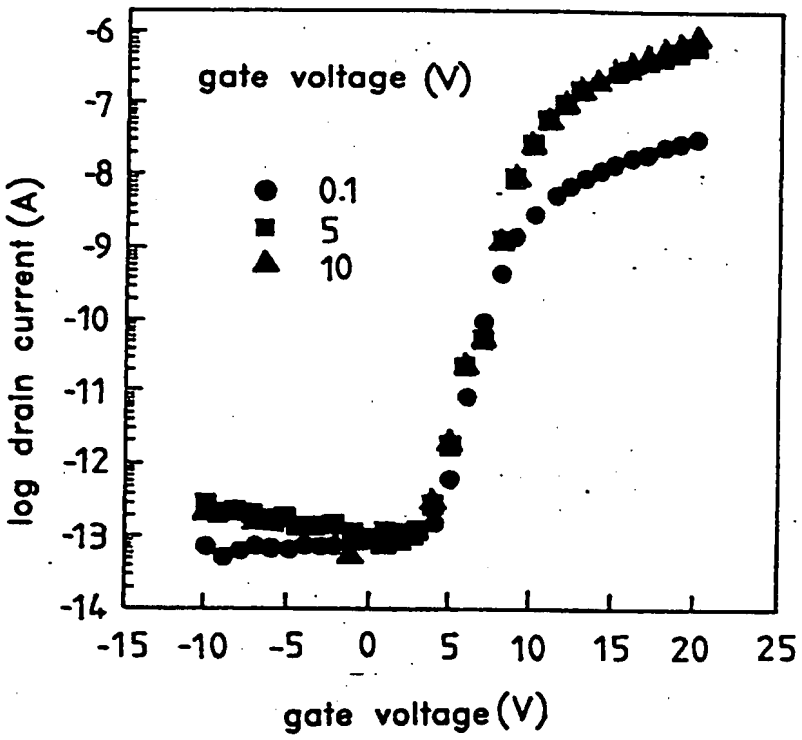

gate voltage (V)
0.1
5
10
log drain current (A)
-6
-7
-8
-9
-10
-11
-12
-13
-14
-15
-10
-5
0
5
10
15
20
25
gate voltage (V)

FIG.8

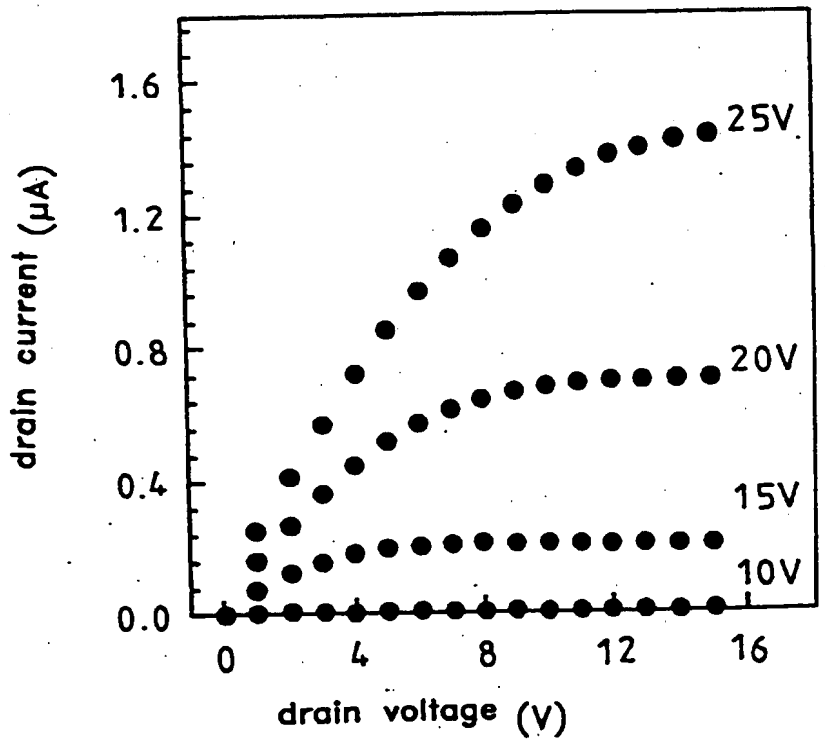
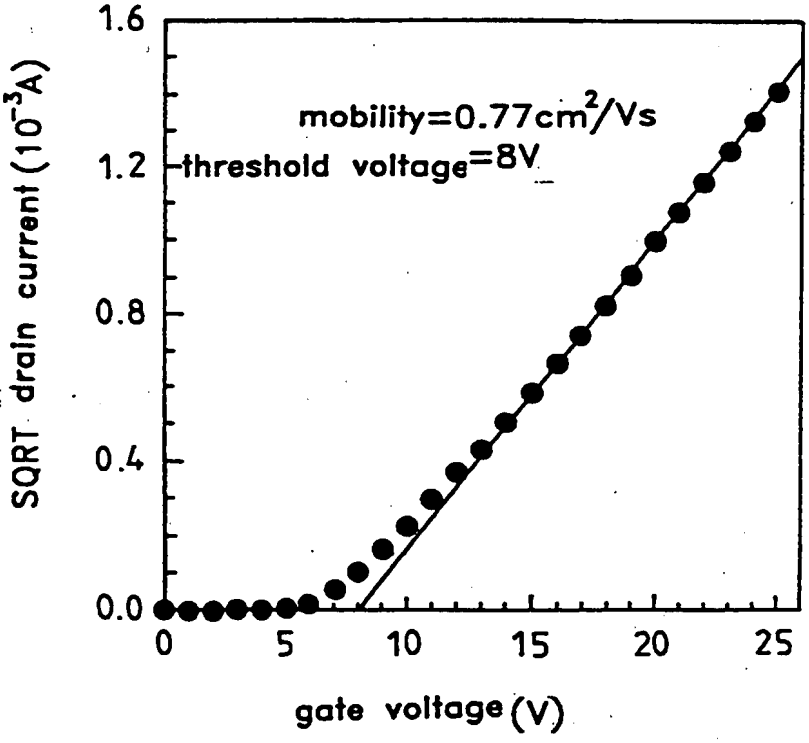

drain current (μA)
1.6
1.2
0.8
0.4
0.0
0
4
8
12
16
drain voltage (V)
25V
20V
15V
10V

FIG.9


1.6
1.2
0.8
0.4
0.0
0
5
10
15
20
25
SQRT drain current (10^{-3}A)
gate voltage (V)
mobility=0.77cm^2/Vs
threshold voltage=8V

GATE INSULATING LAYER HAVING DIAMOND-LIKE CARBON AND THIN FILM TRANSISTOR EMPLOYING THE SAME AND PROCESS FOR MANUFACTURING GATE INSULATING LAYER AND THIN FILM TRANSISTOR

BACKGROUND OF THE INVENTION

Field of the invention

The present invention relates to a technology of a thin film transistor of a liquid crystal device(LCD), and particularly to a gate insulating layer comprising a diamond-like carbon and a thin film transistor with the same and a process for fabricating the gate insulating layer and the thin film transistor.

Description of the Related Art

Generally, a thin film transistor, serving as switching device, includes a normally staggered type of a thin film transistor and an inverted staggered type of the thin film transistor each having a gate electrode vertically separated from a source electrode and a drain electrode via an active layer, i.e., semiconductor layer and a coplanar type of thin film transistor having a gate electrode, a source electrode and a drain electrode all formed on a surface of a semiconductor layer. The active layer is made of one selected from a group consisting of

amorphous silicon, polysilicon, hydrogenated amorphous silicon and chemical semiconductor. Among them, the hydrogenated amorphous silicon a-Si:H is widely used for the thin film transistor(TFT) in view of a good production yield and an easy formation in large scale. A gate insulating layer of thin film transistor with such amorphous silicon layer is double-layered. In the double-layered gate insulating layer, a pin hole generated at a formation of a lower gate insulating layer is removed during a formation of a upper gate insulating layer. Therefore, the yield of the thin film transistor-liquid crystal display(TFT-LCD) employing the double-layered gate insulating layer increases.

There are used Ta_2O_5/SiN_x, Al_2O_3/SiN_x, an atmospheric pressure chemical vapor deposition(APCVD) SiO_2/ a plasma enhanced chemical vapor deposition(PECVD) SiN_x, $SiON/SiN_x$, for the double-layered gate insulating layer of the TFT. Ta_2O_5/SiN_x gate insulating layer is sequentially formed by anode oxidization of Ta and PECVD of SiN_x. Alternatively, both layers can be made by sputtering, achieving high mobility thereof. Because of insolubility of TaO_x to HF or BHF solution, Ta_2O_5/SiN_x decreases an insulating defect, thus increasing a production yield of the TFT employing the same. Since it is, however, to difficult to wet etch the Ta_2O_5/SiN_x, a dry etching should be performed in order to form a contact hole in the gate insulating layer.

SO as to reduce a RC drive delay of a scan line integrated with a gate electrode in TFT array, metal of a low specific resistance is required for the gate electrode. Therefore, instead of chromium, aluminum was used for the gate electrode and a common electrode of an auxiliary capacitance because the specific resistance of the aluminum is about one tenth of that of the chromium. Anode oxidized aluminum Al_2O_3 and SiN_x serve as the double-layered gate insulating layer. However, the manufacturing process of Al_2O_3/SiN_x is complicated.

In TFT using APCVD SiO_2/PECVD SiN_x, another double-layered gate insulating layer, a connection between the APCVD system and the PECVD system is difficult during an in-line process even though the productivity is increased due to the high deposition speed of SiO_2.

As another component of the gate insulating layer there is SiO_xN_y which has smaller mechanical stress, larger optical band gap and stronger hydrophobic than SiN_x. The reproduction of SiO_xN_y formed using PECVD is not good. Accordingly it is rare to use SiO_xN_y as the gate insulating layer for the TFT.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a gate insulating layer for reducing the drawbacks above-mentioned to a maximum and a process for

manufacturing the same.

It is another object of the present invention to provide a thin film transistor employing such gate insulating layer, thus increasing a production yield of the thin film transistor and a process for manufacturing the same.

To accomplish one object, a gate insulating layer of a transistor with a gate electrode and an active layer comprises a diamond-like carbon layer formed between the gate electrode and the active layer. Further, the gate insulating layer comprises a silicon nitride layer formed between the diamond-like carbon layer and the active layer.

A process for forming the gate insulating layer comprises the steps of forming a diamond-like carbon layer between a gate electrode and an active layer. The process further comprises the step of forming a silicon nitride layer on the diamond-like carbon layer after forming the diamond-like carbon layer and before forming the active layer or on the active layer after forming the active layer and before forming the diamond-like carbon layer.

Here, the diamond-like carbon layer is formed by a plasma enhanced chemical vapor deposition. And the silicon nitride layer is also formed by the plasma enhanced chemical vapor deposition. The diamond-like carbon layer is formed using a gas containing carbon element therein such as CH_4, C_2H_6, C_2H_2 or C_3H_8. Also, the diamond-like carbon

layer is formed at 25°C through 400°C.

To accomplish another object, a thin film transistor, comprises a gate electrode; an active layer; and a gate insulating layer at least having a diamond-like carbon layer, formed between the gate electrode and the active layer. The active layer is made of one selected from a group consisting of amorphous silicon, polysilicon, hydrogenated amorphous silicon and compound semiconductor. The gate insulating layer further comprises a silicon nitride layer formed between the diamond-like carbon layer and the active layer. In an inverted staggered type TFT, the gate electrode is formed beneath the gate insulating layer(or the diamond-like carbon layer) and a source electrode is formed on a part of the active layer, and a drain electrode separated from the source electrode, is formed on the same plane as the source electrode. In a normally staggered type, the gate electrode is formed on the gate insulating layer (or the diamond-like carbon layer) and a source electrode is formed beneath a part of the active layer, and a drain electrode separated from the source electrode, is formed on the same plane as the source electrode. In a coplanar type, the gate electrode is formed on the gate insulating layer(or diamond-like carbon layer) and a source electrode is formed on the active layer, and a drain electrode separated from the source electrode, is formed on the same plane as the source electrode.

A process for manufacturing an inverted staggered type TFT comprises the steps of forming a gate electrode on a substrate; forming a gate insulating layer comprising a diamond-like carbon layer, on the substrate including the gate electrode; forming an active layer on the gate insulating layer; and forming a source electrode on a part of the active layer; and forming a drain electrode separated from the source electrode on the same plane as the source electrode. Here, the active layer is made of one selected from a group consisting of amorphous silicon, polysilicon, hydrogenated amorphous silicon and compound semiconductor. The process further comprises the step of forming a silicon nitride layer on the diamond-like carbon layer before forming the active layer.

A process for forming a normally staggered type TFT on a substrate, comprises the steps of forming a source electrode on a part of the substrate; forming a drain electrode separated from the source electrode, on the same plane as the source electrode; forming an active layer on the substrate including the source electrode and the drain electrode; forming a gate insulating layer comprising a diamond-like carbon layer, on the active layer; and forming a gate electrode on the gate insulating layer. The process further comprises the step of forming a silicon nitride layer on the active layer before forming the diamond-like carbon layer.

A process for forming a coplanar type TFT on a substrate, comprises the steps of forming an active layer on the substrate; forming a source electrode on a part of the active layer; forming a drain electrode separated from the source electrode, on the same plane as the source electrode; forming a gate insulating layer between the source electrode and the drain electrode, on another part of the active layer, the gate insulating layer comprising diamond-like carbon layer; and forming a gate electrode on the gate insulating layer. The process further comprises the step of forming a silicon nitride layer on the active layer before forming the diamond-like carbon layer.

Since diamond-like carbon with good insulating property is used as a gate insulating layer, a production yield of a TFT employing the diamond-like carbon increases.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view of an inversely staggered type thin film transistor employing a gate insulating layer comprising a diamond-like carbon layer and silicon nitride layer in accordance with the present invention.

Fig.2 is a sectional view of a normally staggered type thin film transistor employing a gate insulating layer comprising a diamond-like carbon layer and silicon nitride layer in accordance with the present invention.

Fig.3 is a sectional view of a coplanar type thin film transistor employing a gate insulating layer comprising a diamond-like carbon layer and silicon nitride layer in accordance with the present invention.

Fig.4 is a view showing a current to a voltage characteristic of a diamond-like carbon layer used as a gate insulating layer of the TFT.

Fig.5 is a view showing a leakage current characteristic of a diamond-like carbon layer used as a gate insulating layer of the TFT, in response to hydrogen flow used for deposition thereof.

Fig.6 is a view showing an optical band gap of the diamond-like carbon layer used as the gate insulating layer of the TFT.

Fig.7 is a view showing a drain current to a gate voltage characteristic of the hydrogenated amorphous silicon TFT with double-layered gate insulating layer comprising the diamond-like carbon and silicon nitride.

Fig. 8 is a view showing an output feature of hydrogenated amorphous silicon TFT with double-layered gate insulating layer comprising the diamond-like carbon and silicon nitride.

Fig.9 is a view showing an electric field effect mobility μ_{EF} of the hydrogenated amorphous silicon TFT with double-layered gate insulating layer having diamond-like carbon and silicon nitride.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Herein, embodiments of the invention regarding a thin film transistor including a gate insulating layer and a process of manufacturing thereof will be detail described with reference to the drawings:

Fig.1 is a sectional view of an inverted staggered type of thin film transistor(TFT) according to the present invention. A substrate 10 is prepared. The substrate 10 is of a transparent insulating material such as glass or a silicon substrate having an insulating layer thereon. A gate electrode 11 is disposed on a part of the substrate 10. The gate electrode 11 is made of metal such as chromium or aluminum for tapper etch so as to enhance a step coverage of thin film to be formed at a sequential process. On the substrate including the gate electrode 11 is formed a gate insulating layer 12. The gate insulating layer comprises a diamond like-carbon layer 12-1 and a silicon nitride layer 12-2. On the other hand, only diamond like-carbon layer 12-1 can play a role of the gate insulating layer by controlling a process condition of forming the diamond-like carbon layer. For example, when a thickness of the diamond-like carbon layer is thicker than that of the diamond-like carbon layer in the double-layered gate insulating layer, the pin hole is greatly removed. An active layer 13 is arranged on the silicon nitride layer 12-2 of the gate

insulating layer 12, by which a characteristic of the TFT is determined. The active layer is made of amorphous silicon, polysilicon, hydrogenated amorphous silicon or compound semiconductor. In this embodiment, the hydrogenated amorphous silicon is employed as a component of the active layer. Among the active layer, the corresponding portion to the gate electrode 11 is a channel region of the TFT. Low resistance contact regions 14a and 14b for a good ohmic contact characteristic are formed on both ends of the active layer. The low resistance contact regions 14a and 14b both are of highly doped amorphous silicon, highly doped hydrogenated amorphous silicon or highly doped hydrogenated micro-crystal silicon($n^+\mu$ c-si:H). A source electrode 15a and a drain electrode 15b are formed on the active layer 13 and the low resistance contact layers 14a and 14b.

The process for the TFT in Fig.1 will be described below. Metal of chromium or aluminum is deposited on the substrate 10 to form the gate electrode 11. A first gate insulating layer 12-1 of diamond-like carbon is formed on the substrate 10 including the gate electrode 11 by a plasma enhanced chemical vapor deposition(PECVD) using a gas containing a carbon element such as CH_4, C_2H_6, C_2H_2 or C_3H_8. The deposition of diamond-like carbon is carried out in a manner of a self-reducing electric field under 15sccm of CH_4 gas, 0 through 30sccm of H_2 gas, 20sccm of He gas, 25

through 250°C of a substrate temperature, 100W of RF power and 500mTorr of a gas pressure.

Here, the self-reducing electric filed will be explained. Generally, the diamond-like carbon is grown on an electrode to which a plus RF power is applied. If a discharge is made after supplying the plus power to the electrode, on the electrode is formed an ion sheath region caused by a mobility difference between an electron and a charged particle. The ion sheath region has a electric field by a plasma, taking minus voltage. Therefore, because of the electric field by the plasma, a particle charged in plus easily moves toward the electrode with acceleration and on the electrode, an ion bumbardment between the plus charged ion and the minus charged ion is generated, thereby forming the hard diamond-like carbon layer. In case of using the diamond-like carbon as an insulating layer, the ion bombardment destroys the insulating characteristic thereof. Therefore, in order to reduce the ion bombardment, the diamond-like carbon is preferably grown on an electrode which is grounded. This is the self-reducing electric field.

After forming the diamond-like carbon layer 12-1, a second gate insulating layer 12-2 of silicon nitride is deposited on the first gate insulating layer 12-1 of diamond-like carbon. The silicon nitride is deposited in PECVD apparatus under 0.5sccm 0f SiH_4 gas, 28sccm of

ammonia gas, 100sccm of He gas, 300°c of the substrate temperature, 30W of the RF power, 400mTorr of the gas pressure. Thereafter, hydrogenated amorphous silicon and a highly doped hydrogenated amorphous silicon are successively deposited on the second gate insulating layer 12-2 and patterned to form the active layer 13 and the low resistance contact layers 14a and 14b. The hydrogenated amorphous silicon for the active layer 13 is deposited in the PECVD apparatus under 1sccm 0f SiH_4 gas, 200°c of the substrate temperature, 10W of RF power, 200mTorr of gas pressure. A carrier in the active layer 13 of hydrogenated amorphous silicon moves to the interface between the second gate insulating layer 12-2 of silicon nitride and the active layer 13, to form a channel layer of the TFT. Accordingly, a threshold voltage of the TFT is affected by the interface condition therebetween. The highly doped hydrogenated amorphous silicon for the low resistance contact layers 14a and 14b are also deposited in the PECVD apparatus under 0.5sccm 0f SiH_4 gas, 0.01sccm of PH_3 gas, 100sccm of He gas, 200°c of the substrate temperature, 20W of RF power, 200mTorr of gas pressure. The gas flow is controlled by a mass flow controller during the above deposition.

In case where only the diamond-like carbon layer is used as the gate insulating layer, the channel layer is formed between the diamond-like carbon layer and the active

layer by modifying the process condition of the diamond-like carbon layer.

Then, metal is deposited over the substrate and patterned, to form a source electrode 15a and a drain electrode 15b which are overlapped with the active layer 13 via the low resistance contact layers 14a and 14b.

Fig. 2 is a view showing a normally staggered type of the TFT using the double-layered gate insulating layer according to the present invention.

A drain electrode 21 and a source electrode 22 separated from the drain electrode 21 are formed on a substrate 20. An active layer 23 is formed on the resultant in which the source and drain electrodes 21 and 22 are formed. The material of the active layer is one selected from a group consisting of amorphous silicon, hydrogenated amorphous silicon, compound semiconductor and ploysilicon, like in Fig.1. A gate insulating layer comprising the silicon nitride layer 24-1 and the diamond like-carbon layer 24-2 is formed on the active layer 23. The first gate insulating layer 24-1 of silicon nitride contacts with the active layer therebeneath. A gate electrode 25 is formed on the second gate insulating layer 24-2 of diamond-like carbon, with overlapping the source electrode and the drain electrode. The second gate insulating layer 24-2 of diamond-like carbon is formed by the PECVD using a gas containing a carbon element such as CH_4, C_2H_6 C_2H_2 or C_3H_8.

Also, the first gate insulating layer 24-1 of silicon nitride is also formed by the PECVD. The other explanation as to the substrate 20, source electrode/drain electrode 21 and 22, the active layer 23, the gate insulating layer 24-1, 24-2 and the gate electrode 25 is similar to that of Fig.1, which is omitted.

Fig. 3 is a sectional view showing a coplanar type TFT employing the double-layered gate insulating layer according to the present invention.

An active layer 31 is formed on a substrate 30. The material of the active layer is one selected from a group consisting of amorphous silicon, hydrogenated amorphous silicon, compound semiconductor and polysilicion, like in Figs.1 and 2. A drain electrode 32 and a source electrode 33 are formed on a part of the active layer 31. The source electrode 33 is separated from the drain electrode 32. Between the source electrode and the drain electrode, a gate insulating layer 34 comprising the silicon nitride layer 34-1 and the diamond like-carbon layer 34-2 is formed on the active layer 31. The first gate insulating layer 34-1 of silicon nitride contacts with the active layer 31 therebeneath. A gate electrode 35 is formed on the second gate insulating layer 34-2 of diamond-like carbon, with aligning with the gate insulating layer. The second gate insulating layer 34-2 of diamond-like carbon, is formed by the PECVD using a gas containing a carbon element such as

CH_4, C_2H_6, C_2H_2 or C_3H_8. Also, the first gate insulating layer 34-1 of silicon nitride is also formed by the PECVD. The other explanation as to the substrate 30, the drain electrode/ the source electrode 32 and 33, the active layer 31, the gate insulating layer 34-1, 34-2 and the gate electrode 35 is similar to that of Fig.1, which is omitted.

Fig. 4 is a view showing current to voltage characteristic of a diamond-like carbon used as a gate insulating layer of the TFT, in which a deposition temperature is 25°C and 250°C. The diamond-like carbon is deposited to a thickness of 1500Å on a P type silicon wafer with a specific resistance of 10 to 15 $\Omega \cdot$ cm. Aluminum is deposited in 1mm thickness on the diamond like-carbon by a thermal deposition in a vacuum, forming a MIS(metal insulator semiconductor). Then the characteristic of a current to a voltage of the diamond-like carbon layer is measured using Kithely electrometer 617. In Fig.4, a breakdown voltage of the diamond-like carbon layer is 3MV and the current density thereof is 10^{-10} A/cm^2 at electric field of 1MV/cm. On the other hand, as the deposition temperature increases, the current density of the diamond-like carbon layer decreases and the breakdown voltage thereof increases.

Fig.5 is a view showing a leakage current characteristic of a diamond-like carbon used as a gate insulating layer of the TFT, in response to a hydrogen flow

used for a deposition thereof. In Fig.5, when the hydrogen flow is 4sccm or less, the leakage current density of the diamond-like carbon is 10^{-9}A/㎠ or less, showing a good insulating property. The reason is that the diamond-like carbon layer is more closely fine by a self-heating effect. That is, since the deposition of diamond-like carbon is carried out while increasing the temperature of the substrate on which the diamond-like carbon is formed, a diffusion coefficient of the diamond-like carbon increases, enhancing the insulating property thereof. However, since very high temperature makes the structure of the diamond-like carbon layer change and thus transforms the diamond-like carbon layer into a different material, a proper temperature is required. In view of Figs 3 and 4, we can easily acknowledge that the insulating characteristic of the diamond like-carbon layer is closely related to the deposition temperature thereof and the hydrogen flow used in the deposition process. One of other advantages of the diamond-like carbon is that the diamond-like carbon can be grown at room temperature, which results from the self-heating effect.

Fig. 6 shows an optical band gap of the diamond-like carbon layer used as the gate insulating layer of the TFT. The diamond-like carbon is deposited on a corning (R.T.M.) 7059 glass and an optical absorption coefficient α of the diamond-like carbon is measured by UV(ultra

violet)/VIS(visible) spectrometer. The optical band gap is achieved using the optical absorption coefficient α from the following equation.

$$(\alpha h \upsilon)^{1/2} = B(E-E_g^{opt})$$

where, B is a constant showing a slope of a graph in Fig. 6, $h\upsilon$ is an optical energy of an incident light, α is optical absorption coefficient and E_g^{opt} is the optical band gap.

Referring to Fig. 6, the optical band gap of the diamond-like carbon is 4.25eV, so the diamond like-carbon can be used as the insulating layer.

Fig. 7 is a view showing a drain current to a gate voltage characteristic of the hydrogenated amorphous silicon TFT with double-layered gate insulating layer comprising the diamond-like carbon and silicon nitride. In Fig. 7, a subthreshold voltage slope of the diamond-like carbon is about 0.36V/dec and ratio of on current to off current is 10^6 or more.

Fig.8 shows an output feature of hydrogenated amorphous silicon TFT with the double-layered gate insulating layer comprising the diamond-like carbon and the silicon nitride. The diamond-like carbon layer, the silicon nitride layer, the active layer and the low resistance contact layers are 1500Å, 3500 Å, 1500Å and 500 Å, respectively. The diamond-like carbon is deposited under 15sccm of CH_4 gas, 1sccm of H_2 gas, 20sccm of He gas, 250 ℃

of the substrate temperature, 100W of RF power and 500mTorr of gas pressure. The silicon nitride layer 12-2 is deposited under 0.5sccm of SiH_4 gas, 28sccm of ammonia gas, 100sccm of He gas, 300℃ of the substrate temperature, 30W of the RF power and 400mTorr of the gas pressure. The deposition condition of the active layer 13 is as follows: a flow rate of SiH_4 gas is 1sccm, the substrate temperature is 200℃, the RF power is 10W and the gas pressure is 200mTorr. The deposition condition of the low resistance contact layers is as follows: the flow rate of SiH_4 gas is 0.5sccm, the flow rate of PH_3 gas is 0.01sccm, the flow rate of He gas is 100sccm, the substrate temperature is 200℃, the RF power is 20W and the gas pressure is 200mTorr. The ratio of channel width W to channel length L is 60㎛/30㎛. When the gate voltage is 20V, the drain current is saturated at about 0.7×10^{-6}A at which the drain voltage is about 9V.

Fig. 9 shows an electric field effect mobility μ_{EF} of the hydrogenated amorphous silicon TFT with double-layered gate insulating layer having the diamond-like carbon and the silicon nitride. The electric field effect mobility μ_{EF} of the hydrogenated amorphous silicon TFT is calculated from the following equation.

$$I_D=[\mu_{EF}(W/L)C_i(V_G-V_{TH})V_D]^{1/2}$$

Wherein, I_D is a drain current, C_i is a capacitance of the gate insulating layer, V_{TH} is a threshold voltage of

TFT and V_D is a drain voltage.

The threshold voltage V_{TH} calculated is about 8V, and the electric field effect mobility μ_{EF} is about 0.77cm^2/Vs.

In the present embodiment, the diamond-like carbon layer or the diamond-like carbon/silicon nitride layer serves as the gate insulating layer of the TFT. However, the diamond-like carbon layer or the diamond-like carbon/silicon nitride can also used as any insulating layer of the semiconductor device such as an insulating layer between the substrate and a conductor formed on the substrate or between lower conductor and upper conductor. Also, the diamond-like carbon layer or the diamond-like carbon/silicon nitride can be applied to the amorphous silicon TFT, the polysilicon TFT and the compound semiconductor TFT.

The diamond-like carbon layer is used as the gate insulating layer with a good insulating property. Accordingly, the insulating layer of diamond-like carbon greatly contributes to realize the high definition TFT-LCD(liquid crystal display). Also, since the diamond-like carbon layer can be formed by PECVD and the silicon nitride layer is formed by PECVD, it is easy to interconnect the diamond-like carbon layer process system to the silicon nitride layer process system. The diamond-like carbon layer can be formed using a gas containing a carbon element such as CH_4, C_2H_6, C_2H_2 or C_3H_8. Accordingly, amorphous or

polysilicon TFT with the good electrical property is possibly manufactured because the carbon element is less sensitive to the active layer than the oxygen element.

While the present invention has been particularly shown and described with reference to particular embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be effected therein without departing from the spirit and scope of the prevent invention as defined by the appended claims.

What is claimed is:

1. A gate insulating layer of a transistor with a gate electrode and an active layer, comprising a diamond-like carbon layer formed between said gate electrode and said active layer.

2. A gate insulating layer in claim 1, further comprising a silicon nitride layer formed between said diamond-like carbon layer and said active layer.

3. A thin film transistor, comprising:

a gate electrode;

an active layer; and

a gate insulating layer comprising a diamond-like carbon layer, formed between said gate electrode and said active layer.

4. A thin film transistor in claim 3, wherein said active layer is of one selected from a group consisting of amorphous silicon, polysilicon, hydrogenated amorphous silicon and compound semiconductor.

5. A thin film transistor in claim 3, wherein said gate insulating layer further comprises a silicon nitride layer formed between said diamond-like carbon layer and said

active layer.

6. A thin film transistor in claim 4, wherein said gate insulating layer further comprises a silicon nitride layer formed between said diamond-like carbon layer and said active layer.

7. A thin film transistor in claim 6, wherein said diamond-like carbon layer, said silicon nitride layer and said active layer of said hydrogenated amorphous silicon are 1500Å, 3500 Å and 1500 Å, respectively in thickness.

8. A thin film transistor in claim 3, wherein said gate electrode is formed beneath said gate insulating layer and further comprising:

a source electrode formed on a part of said active layer; and

a drain electrode formed separated from said source electrode, on the same plane as said source electrode.

9. A thin film transistor in claim 5, wherein said gate electrode is formed beneath said diamond-like carbon layer and further comprising:

a source electrode formed on a part of said active layer; and

a drain electrode formed separated from said source

electrode, on the same plane as said source electrode.

10. A thin film transistor in claim 3, wherein said gate electrode is formed on said gate insulating layer and further comprising:

a source electrode formed beneath a part of said active layer; and

a drain electrode formed separated from said source electrode, on the same plane as said source electrode.

11. A thin film transistor in claim 5, wherein said gate electrode is formed on said diamond-like carbon layer and further comprising:

a source electrode formed beneath a part of said active layer; and

a drain electrode formed separated from said source electrode, on the same plane as said source electrode.

12. A thin film transistor in claim 3, wherein said gate electrode is formed on said gate insulating layer and further comprising:

a source electrode formed on said active layer; and

a drain electrode formed separated from said source electrode, on the same plane as said source electrode.

13. A thin film transistor in claim 5, wherein said gate

electrode is formed on said diamond-like carbon layer and further comprising:

a source electrode formed on said active layer; and

a drain electrode formed separated from said source electrode, on the same plane as said source electrode.

14. A process for forming a gate insulating layer of a transistor with a gate electrode and an active layer, comprising the step of forming a diamond-like carbon layer between said gate electrode and said active layer.

15. A process in claim 14, further comprising the step of forming a silicon nitride layer on said diamond-like carbon layer after forming said diamond-like carbon layer and before forming said active layer.

16. A process in claim 14, further comprising the step of forming a silicon nitride layer on said active layer after forming said active layer and before forming said diamond-like carbon layer.

17. A process in claim 14, wherein said diamond-like carbon layer is formed by a plasma enhanced chemical vapor deposition.

18. A process in claim 15, wherein both said diamond-like

carbon layer and said silicon nitride layer are formed by a plasma enhanced chemical vapor deposition.

19. A process in claim 16, wherein both said diamond-like carbon layer and said silicon nitride layer are formed by a plasma enhanced chemical vapor deposition.

20. A process in claim 17, wherein said diamond-like carbon layer is formed using a gas containing carbon element therein.

21. A process in claim 18, wherein said diamond-like carbon layer is formed using a gas containing carbon element therein.

22. A process in claim 20, wherein said gas is one selected from a group consisting of CH_4, C_2H_6, C_2H_2 and C_3H_8.

23. A process in claim 21, wherein said gas is one selected from a group consisting of CH_4,C_2H_6, C_2H_2 and C_3H_8.

24. A process in claim 14, wherein said diamond-like carbon layer is formed at 25°C through 400°C.

25. A process for forming a thin film transistor on a substrate, comprising the steps of:

forming a gate electrode on said substrate;

forming a gate insulating layer comprising a diamond-like carbon layer, on said substrate including said gate electrode;

forming an active layer on said gate insulating layer; and

forming a source electrode on a part of said active layer; and

forming a drain electrode separated from said source electrode on the same plane as said source electrode.

26. A process in claim 25, wherein said active layer is of one selected from a group consisting of amorphous silicon, polysilicon, hydrogenated amorphous silicon and compound semiconductor.

27. A process in claim 25, further comprising the step of forming a silicon nitride layer on said diamond-like carbon layer before forming said active layer.

28. A process in claim 26, further comprising the step of forming a silicon nitride layer on said diamond-like carbon layer before forming said active layer.

29. A process for forming a thin film transistor on a substrate, comprising the steps of:

forming a source electrode on a part of said substrate;

forming a drain electrode separated from said source electrode, on the same plane as said source electrode;

forming an active layer on said substrate including said source electrode and said drain electrode;

forming a gate insulating layer comprising a diamond-like carbon layer, on said active layer; and

forming a gate electrode on said gate insulating layer.

30. A process in claim 29, wherein said active layer is of one selected from a group consisting of amorphous silicon, polysilicon, hydrogenated amorphous silicon and compound semiconductor.

31. A process in claim 29, further comprising the step of forming a silicon nitride layer on said active layer before forming said diamond-like carbon layer.

32. A process for forming a thin film transistor on a substrate, comprising the steps of :

forming an active layer on said substrate;

forming a source electrode on a part of said active layer;

forming a drain electrode separated from said source

electrode, on the same plane as said source electrode;

forming a gate insulating layer between said source electrode and said drain electrode, on another part of said active layer, said gate insulating layer comprising diamond-like carbon layer; and

forming a gate electrode on said gate insulating layer.

33. A process in claim 32, wherein said active layer is of one selected from a group consisting of amorphous silicon, polysilicon, hydrogenated amorphous silicon and compound semiconductor.

34. A process in claim 32, further comprising the step of forming a silicon nitride layer on said active layer before forming said diamond-like carbon layer.

The Patent Office

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Claims searched:	All	**Date of search:**	23 February 1998

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H1K(KJAD,KCAA)

Int Cl (Ed.6): H01L

Other: ON LINE,W.P.I.

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X	GB2254733 A	KOBE SEIKO SHO	1,3,14,32 at least
X	GB2243949 A	KOBE SEIKO SHO	1,3,14 at least
X	US 5523588	KOBE SEIKO SHO	1,3,14,32 at least
X	Pat.Abs.of Jp.Vol.7,No.255(E210),12/11/83,Page133,and JP58-141572,SUWA SEIKOSHA		1,3,14 at least

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